AN EQUIVALENT CIRCUIT INTERPRETATION OF ANTIDERIVATIVE ANTIALIASING

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ABSTRACT

The recently proposed antiderivative antialiasing (ADAA) technique for stateful systems involves two key features: 1) replacing a nonlinearity in a physical model or virtual analog simulation with an antialiased nonlinear system involving antiderivatives of the nonlinearity and time delays and 2) introducing a digital filter in cascade with each original delay in the system. Both of these features introduce the same delay, which is compensated by adjusting the sampling period. The result is a simulation with reduced aliasing distortion. In this paper, we study ADAA using equivalent circuits, answering the question: "Which electrical circuit, discretized using the bilinear transform, yields the ADAA system?" This gives us a new way of looking at the stability of ADAA and how introducing extra filtering distorts a system's response. We focus on the Wave Digital Filter (WDF) version of this technique.

1. INTRODUCTION

Aliasing mitigation is a central issue in virtual analog modeling. The simplest way to mitigate aliasing is to oversample [1]. Because this can be expensive, research often seeks to reduce oversampling requirements [2]. The earliest work on antialising in virtual analog considered antialiased oscillators [3], a research thread which continues today [4, 5]. These techniques have also been applied to antialias memoryless nonlinear waveshapers [6]. Parker *et al.* recently proposed an antialiasing technique called antiderivative antialiasing (ADAA), which involves approximating the process of upsampling, distorting, and downsampling using antiderivatives of a nonlinear waveshaping functions [7], originally using 1st- and 2nd-order filter kernels. 1st-, 2nd-, and 3rd-order filter kernels are reformulated and discussed by Bilbao *et al.* in [8]. Esqueda *et al.* showed these techniques applied to case studies: the classic Lockhart and Serge wavefolder circuits [9]. Alternative kernels optimized for spectral flatness are discussed in [10].

For physical systems with memory/state, antialiasing techniques are quite complex [11]. [7] showed one example of how to apply ADAA to a stateful system. Paschou *et al.* showed [12] how to apply this technique to the classic Moog ladder filter [13–16]. Holters formalized this further to handle circuits written in the state-space formalism, using 1st-order ADAA [17, 18]. Carson extended this to 2nd-order ADAA and proposed a way to handle two-port nonlinearities [19]. Albertini *et al.* [20] applied ADAA to the Wave Digital Filter (WDF) [21–23] modeling formalism.

In applying ADAA to stateful systems, we introduce filters into feedback paths, so must consider stability. Holters [17, 18] showed that the 1st-order ADAA filter in a state-space model preserves stability, since for a linear system the mapping can be expressed as an inwards contraction of the z-plane.

This raises the question: If we can analyze this part of ADAA as a deformation of the z-plane, could we also analyze it as a deformation of the original continuous-time circuit? This paper finds the equivalent circuits corresponding to capacitors and inductors treated with 1st- and 2nd-order ADAA filters.

WDF modeling involves replacing electronic circuit elements with discrete-time models [21]. Equivalent circuits appear throughout WDF theory, for instance in deriving scattering matrices of multiport adaptors [23], studies of higher-order linear multistep discretization methods [24], interpreting different discretization methods as the addition of electrical circuits [2], and Runge-Kutta methods [25, 26]. This paper hence connects to a tradition of using equivalent electronic circuits to analze digital systems.

In the rest of this paper, we review some preliminaries (§2), convert an ADAA'd capacitor (§3) and inductor (§4) to electronic circuits, discuss (§5), and conclude (§6). Two Appendices (§§A–B) present an alternate synthesis perspective, and illustrate how to apply Brune synthesis (to the 1st-order ADAA'd capacitor).

2. REVIEW

2.1. Wave Digital Filters

The Wave digital Filter (WDF) [21] approach to circuit modeling involves two key features. First, a transformation at every port of the circuit of the port voltage v and port current i to an "incident wave" a and "reflected wave"[1] according to

$$\begin{array}{l} a = v + Z_\text{P} i \\ b = v - Z_\text{P} i \end{array} \iff \begin{array}{l} v = (a+b)/2 \\ i = (a-b)/2Z_\text{P} \end{array}, \tag{1}$$

where $Z_\text{P} \neq 0$ is a free parameter called "port resistance." Second, derivatives in reactance (inductor and capacitor) constitutive equations, represented by the Laplace transform variable s, are approximated in discrete-time using the bilinear transform (BLT) [27, 28]

$$s = \frac{2}{T}\frac{1-z^{-1}}{1+z^{-1}} \iff z = \frac{2+Ts}{2-Ts} \quad \text{or} \quad z^{-1} = \frac{2-Ts}{2+Ts}, \tag{2}$$

where z^{-1} is the discrete delay operator of the Z-transform and $T = 1/f_\text{s}$ is the sampling period (reciprocal of the sampling rate f_s). A full review is given in the literature [21–23].

2.2. Antiderivative Antialiasing (ADAA)

Consider a memoryless nonlinear function that produces an output $y(t)$ from an input $x(t)$, of the form $y(t) = F_0(x(t))$. Nth-order ADAA involves replacing F_0 with a function of its first N

[1] We use classic "voltage waves," though many other wave types exist.

antiderivatives, F_1 through F_N, that form a finite-difference approximation. For instance, 1st-order ADAA is

$$y[n] = \left(F_1(x[n]) - F_1(x[n-1])\right) / \left(x[n] - x[n-1]\right) \quad (3)$$

and 2nd-order ADAA is

$$y[n] = \frac{2}{x[n]-x[n-1]} \left(\frac{F_2(x[n]) - F_2(x[n-1])}{x[n]-x[n-1]} \dots - \frac{F_2(x[n-1]) - F_2(x[n-2])}{x[n-1]-x[n-2]} \right) . \quad (4)$$

Various strategies are given for how to handle the case of numerical ill-conditioning [7, 8, 19], e.g., $x[n] \approx x[n-1]$.

For small signal levels, or a linear circuit [19], 1st- and 2nd order ADAA are equivalent to the FIR filters

$$H_{\text{AA},1}(z) = Y(z)/X(z) = (1 + z^{-1})/2 \quad (5)$$

$$H_{\text{AA},2}(z) = Y(z)/X(z) = (1 + z^{-1} + z^{-2})/3 . \quad (6)$$

When applying ADAA to stateful systems, the delays are also cascaded with one of these filters (5)–(6), to match the delay that the the normally memoryless nonlinearity experiences [17–20]. In this paper, we study 1st- and 2nd-order ADAA, in the linear case only, investigating their effect on linear reactances in circuits.

2.3. Positive real immitances and Brune network synthesis

An immitance (impedance or admittance) $W(s)$ is called "positive real" (p.r.) if it has the following properties

$$\Re\{W(s)\} > 0 \quad \text{if} \quad \Re\{s\} > 0 \quad (7)$$

$$\Im\{W(s)\} = 0 \quad \text{if} \quad \Im\{s\} = 0 . \quad (8)$$

A p.r. immitance written as a ratio of polynomials in s must have all real and positive coefficients, with possibly only a leading or trailing coefficient in the numerator or denominator equal to zero, with the order of the numerator and denominator differing by no more than one [29]. Crucially, a p.r. immitance is realizable as a one-port circuit network of passive linear elements: resistors, capacitors, inductors, transformers.

One way of finding this circuit is Brune's method [29, 30]. It starts with the so-called "Foster preamble," which involves successively removing series or shunt reactances (or pairs of reactances) from an immitance function, reducing the order of its numerator or denominator each time. Upon arriving at a circuit with no poles or zeros at $s = 0$ or $s = \infty$, you then remove the minimum resistance or conductance, then more complicated multi-element two-ports involving reactances and transformers; the process repeats until nothing is left. In this paper, we coincidentally never need to extract any multi-element two-ports.

3. ANTIALIASED CAPACITOR AS CIRCUIT

In this section, we'll derive electrical circuits corresponding to 1st- and 2nd-order ADAA filters applied to a capacitor.

3.1. WDF Leaf Capacitor

First, we'll consider a "adapted" WDF capacitor [21, 22].

The constitutive equation for a time-invariant capacitor is

$$V(s) = (1/Cs)I(s) , \quad (9)$$

where V is the port voltage, I is the port current, C is the capacitance, and s is the Laplace differentiation variable. Put another way, the capacitor's impedance $Z_{\text{C}}(s)$ is

$$Z_{\text{C}}(s) = V(s)/I(s) = 1/Cs . \quad (10)$$

An impedance $Z(s) = \frac{V(s)}{I(s)}$ is related to a wave-domain reflectance $R(s) = \frac{B(s)}{A(s)}$, where the wave variables are defined as in (1), by

$$R(s) = \frac{B(s)}{A(s)} = \frac{Z_{\text{C}}(s) - Z_{\text{P}}}{Z_{\text{C}}(s) + Z_{\text{P}}} \quad (11)$$

or conversely

$$Z(s) = \frac{V(s)}{I(z)} = \frac{1 + R(s)}{1 - R(s)} Z_{\text{P}} . \quad (12)$$

Using (11), we can find the continuous time reflectance as

$$R_{\text{C}}(s) = \frac{B(s)}{A(s)} = \frac{1 - CZ_{\text{P}}s}{1 + CZ_{\text{P}}s} . \quad (13)$$

The BLT (2) converts this to a discrete-time reflectance

$$R_{\text{C}}(z) = \frac{B(z)}{A(z)} = \frac{(T - 2CZ_{\text{P}}) + (T + 2CZ_{\text{P}})z^{-1}}{(T + 2CZ_{\text{P}}) + (T - 2CZ_{\text{P}})z^{-1}} . \quad (14)$$

To "adapt" this WDF capacitor—that is, to set the leading numerator term $T - 2CZ_{\text{P}}$ to zero—we set the free port resistance parameter to $Z_{\text{P}} = \frac{T}{2C}$, giving an adapted discrete-time reflectance

$$R_{\text{C}}(z) = z^{-1} . \quad (15)$$

3.2. 1st-order ADAA

1st-order ADAA puts an additional filter $H_{\text{AA},1}(z)$, as defined in Eqn. (5), in cascade with this reflectance. This cascade yields

$$\tilde{R}_{\text{C}}(z) = R_{\text{C}}(z) H_{\text{AA},1}(z) = \left(z^{-1} + z^{-2}\right)/2 . \quad (16)$$

Now we arrive at a central question of the paper: Which analog circuit, discretized with the BLT, would have yielded the discrete-time reflectance (16)? We can approach this question by running the steps that we took to get from the original capacitor circuit to the adapted WDF capacitor, in reverse.

First, we comment on the port resistance. Along with treating the nonlinearity and filtering the states with $H_{\text{AA},1}(z)$, Albertini *et al.* [20] adopt the same approach of Holters [17, 18], replacing the sampling period T with $\tilde{T} = \frac{3}{2}T$ (or, the sampling rate $\tilde{f}_{\text{s}} = \frac{2}{3} f_{\text{s}}$), as part of synchronizing the states with the nonlinearities that have picked up some extra delay.

We can observe that the only place T really appears in WDFs is the port resistance of an adapted capacitor ($Z_{\text{P}} = \frac{T}{2C}$) or an adapted capacitor ($Z_{\text{P}} = \frac{2L}{T}$). In each case, it appears in the same expression as the capacitance C or inductance L, which also only occur in the port resistance equations. So, is there any particular reason that we should interpret the adjustment as a change to T (resp. f_{s}) instead of an adjustment to C or L? For the moment, we will hedge our bets, and replace the port resistance $Z_{\text{P}} = T/2C$ with a modified port resistance $\tilde{Z}_{\text{P}} = \tilde{T}/2\tilde{C}$, where both the sampling period $\tilde{T}$ and capacitance $\tilde{C}$ have been modified in some way, without making any particular claim about which one (or both?) is modified, and *without* defining $\tilde{T} = \frac{3}{2}T$.

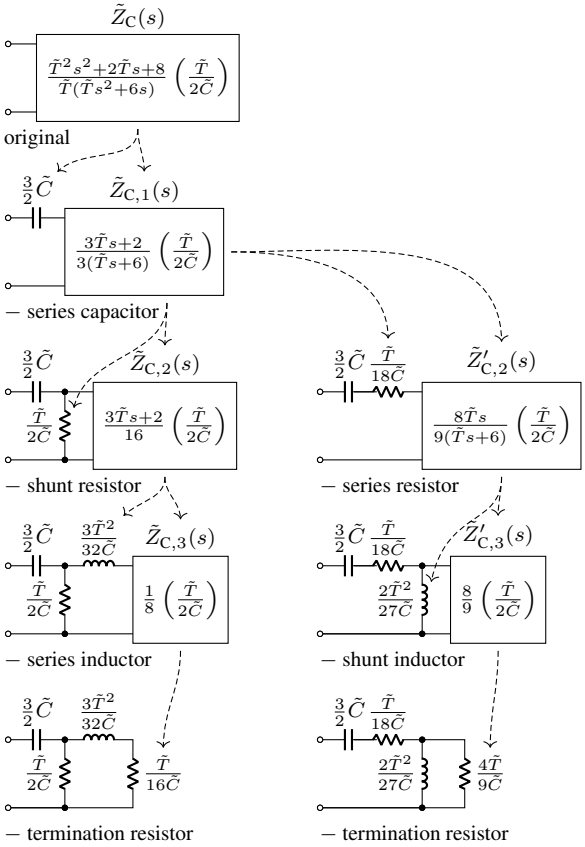

Figure 1: *Synthesizing two possible circuits from the continuous-time capacitor impedance resulting from* 1*st-order ADAA.*

Now, we can use the inverse BLT (2) on (16), again replacing T by $\tilde{T}$, to obtain a continuous-time reflectance

$$\tilde{R}_{\mathrm{C}}(s) = \frac{\tilde{B}(s)}{A(s)} = \frac{4 - 2\tilde{T}s}{4 + 4\tilde{T}s + \tilde{T}^2 s^2}\,. \tag{17}$$

Now, we can use (12) to find the continuous-time impedance

$$\tilde{Z}_{\mathrm{C}}(s) = \frac{8 + 2\tilde{T}s + \tilde{T}^2 s^2}{6\tilde{T}s + \tilde{T}^2 s^2}\left(\frac{\tilde{T}}{2\tilde{C}}\right). \tag{18}$$

Even before finding a circuit that goes along with this impedance, we can see that it represents a passive impedance, because it is p.r..

Unlike in the forwards direction, where we associated a capacitor of value C with an impedance $Z_{\mathrm{C}} = \frac{1}{Cs}$ by inspection (since the relationship is true by definition!), here we are faced with a much more complicated *network synthesis* problem to solve: Which electrical circuit has the impedance $\tilde{Z}_{\mathrm{C}}(s)$ shown in (18)?

We can answer this question with the classical Brune synthesis [29, 30] reviewed in §2.3. Fig. 1 shows two possible outcomes of Brune synthesis on (18). A detailed walkthrough of this procedure is given in Appendix A. The two possible networks that result each comprise two resistors, a capacitor, and an inductor.

An alternative approach is given in Appendix B. This derivation relies on an intuitive recognition of known WDF elements, but yields a network that involves an uncommon circuit element—a circulator—so it will likely be less useful that the derivation yielding a circuit comprising only one-port RLC elements.

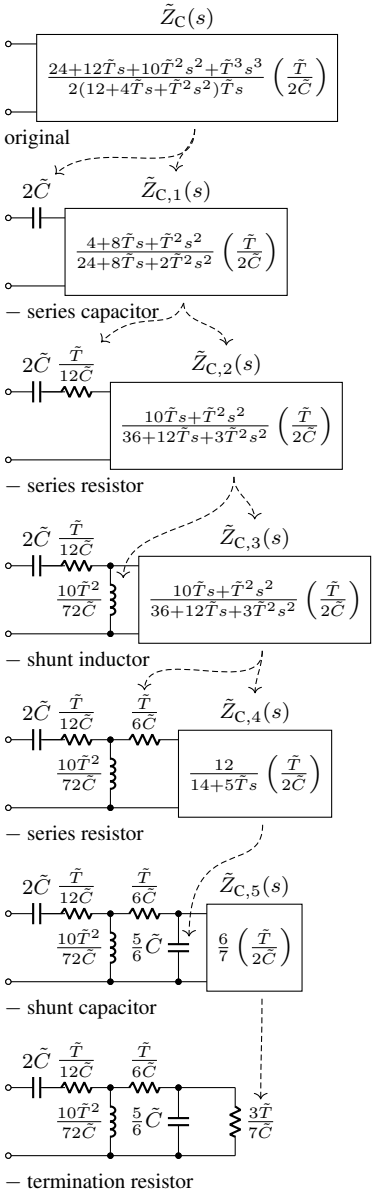

Figure 2: *Synthesizing circuit from capacitor impedance resulting from* 2*nd-order ADAA.*

3.3. 2nd-order ADAA

2nd-order ADAA instead puts the filter $H_{\mathrm{AA},2}(z)$, as defined in Eqn. (6), in cascade with the reflectance (15), yielding

$$\tilde{R}_{\mathrm{C}}(z) = R_{\mathrm{C}}(z) H_{\mathrm{AA},2}(z) = (z^{-1} + z^{-2} + z^{-3})/3\,. \tag{19}$$

Just as in the 1st-order case, we obtain a continuous-time reflectance

$$\tilde{R}_{\mathrm{C}}(s) = \frac{\tilde{B}(s)}{A(s)} = \frac{24 - 12\tilde{T}s + 2\tilde{T}^2 s^2 - \tilde{T}^3 s^3}{24 + 36\tilde{T}s + 18\tilde{T}^2 s^2 + 3\tilde{T}^3 s^3}\,. \tag{20}$$

Using (12), we find the continuous-time impedance

$$\tilde{Z}_{\mathrm{C}}(s) = \frac{24 + 12\tilde{T}s + 10\tilde{T}s^2 + \tilde{T}^3 s^3}{(24 + 8\tilde{T}s + 2\tilde{T}^2 s^2)\tilde{T}s}\left(\frac{\tilde{T}}{2\tilde{C}}\right). \tag{21}$$

Brune synthesis yields the circuit shown at the bottom of Fig. 2.

4. ANTIALIASED INDUCTOR AS CIRCUIT

The derivation for the WDF inductor with 1st or 2nd-order ADAA proceeds similarly to the capacitor.

4.1. WDF Leaf Inductor

The constitutive equation for a time-invariant inductor is

$$V(s) = Ls\, I(s)\,, \tag{22}$$

where L is the inductance. Its impedance is

$$Z_{\mathrm{L}}(s) = V(s)/I(s) = Ls\,. \tag{23}$$

Using the BLT (2), (11), and setting port resistance $Z_{\mathrm{P}} = \frac{2L}{T}$ to adapt the inductor gives us a discrete-time reflectance

$$R_{\mathrm{L}}(z) = -z^{-1}\,. \tag{24}$$

4.2. 1st-order

For the inductor, 1st-order ADAA (defining $Z_{\mathrm{P}} = \frac{2\tilde{L}}{\tilde{T}}$) yields the reflectance

$$\tilde{R}_{\mathrm{L}}(z) = R_{\mathrm{L}}(z)H_{\mathrm{AA},1}(z) = -\left(z^{-1} + z^{-2}\right)/2\,. \tag{25}$$

The inverse BLT (2) yields the continuous-time reflectance

$$\tilde{R}_{\mathrm{L}}(s) = \frac{\tilde{B}(s)}{\tilde{A}(s)} = \frac{-4 + 2\tilde{T}s}{4 + 4\tilde{T}s + \tilde{T}^2s^2}\,. \tag{26}$$

Now, we can use (12) to find the continuous-time impedance

$$\tilde{Z}_{\mathrm{L}}(s) = \frac{(6s + \tilde{T}s^2)\tilde{T}}{8 + 2\tilde{T}s + s^2\tilde{T}^2}\left(\frac{2\tilde{L}}{\tilde{T}}\right)\,. \tag{27}$$

Brune synthesis yields the two circuits shown in Fig. 3.

4.3. 2st-order ADAA

For the inductor, 2nd-order ADAA yields the reflectance

$$\tilde{R}_{\mathrm{L}}(z) = R_{\mathrm{L}}(z)H_{\mathrm{AA},2}(z) = -\left(z^{-1} + z^{-2} + z^{-3}\right)/3\,. \tag{28}$$

The inverse BLT (2) yields the continuous-time reflectance

$$\tilde{R}_{\mathrm{L}}(s) = \frac{\tilde{B}(s)}{\tilde{A}(s)} = \frac{-24 + 12\tilde{T}s - 2\tilde{T}^2s^2 + \tilde{T}^3s^3}{24 + 36\tilde{T}s + 18\tilde{T}^2s^2 + 3\tilde{T}^3s^3}\,. \tag{29}$$

Now, we can use (12) to find the continuous-time impedance

$$\tilde{Z}_{\mathrm{L}}(s) = \frac{(24 + 8\tilde{T}s + 2\tilde{T}^2s^2)\tilde{T}s}{24 + 12\tilde{T}s + 10\tilde{T}^2s^2 + \tilde{T}^3s^3}\left(\frac{2\tilde{L}}{\tilde{T}}\right)\,. \tag{30}$$

Brune synthesis yields the dual of the circuit shown in Fig. 2.

5. DISCUSSION

5.1. Duals

The ADAA'd capacitor and inductors are duals, just like standard capacitors and inductors. That is, all of the following pairs trade places: currents and voltages, capacitances and inductances, series and parallel connections, and impedances and admittances.

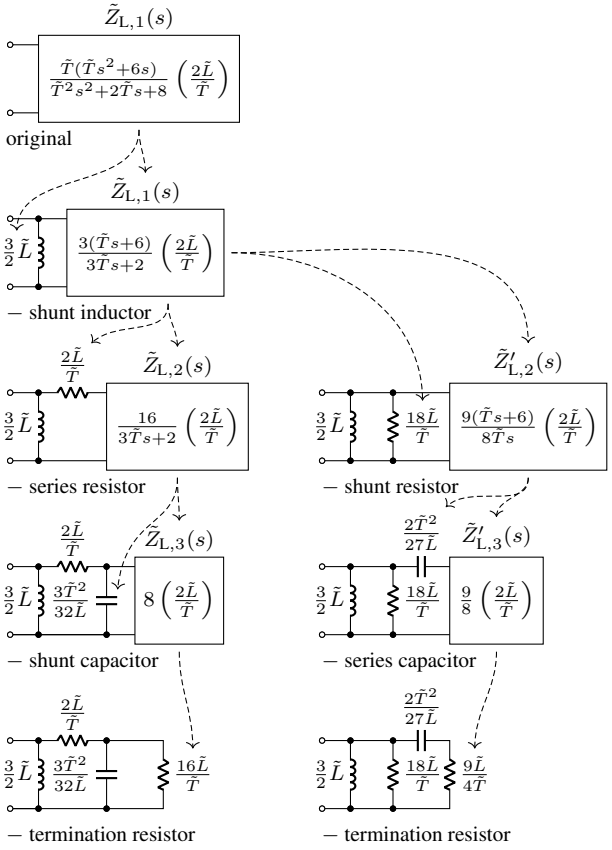

Figure 3: *Synthesizing two possible circuits from the continuous-time inductor impedance resulting from* 1*st-order ADAA.*

5.2. Stability

In all of the presented circuits, since $\tilde{T} > 0$, positive capacitances $C > 0$ (resp. inductances $L > 0$) treated with 1st- and 2nd-order ADAA yield networks with positive electrical elements, meaning that these networks are passive, and hence stable. We can also confirm that the networks are passive because their impedances are all p.r. This confirms Holters' reasoning [17, 18] (on the z-plane), extending it also to 2nd-order ADAA.

5.3. Asymptotic circuits

Do these circuits, like many digital models, converge to anything in particular as the $f_{\mathrm{s}} \longrightarrow \infty$ ($T \longrightarrow 0$)? In all of the presented circuits, the first extracted reactance does not depend at all on $\tilde{T}$. In the 1st-order ADAA'd cases, it is easy to see which resistors turn into shorts and which into open circuits as T shrinks, which shows that the capacitor converges to a capacitor $\frac{3}{2}\tilde{C}$ and the inductor to an inductance $\frac{3}{2}\tilde{L}$. Considering also that inductors look like shorts near DC, and capacitors like open circuits, we can see that for 2nd-order ADAA, the capacitor converges to a capacitor $2\tilde{C}$ and the inductor to an inductance $2\tilde{L}$ as T shrinks.

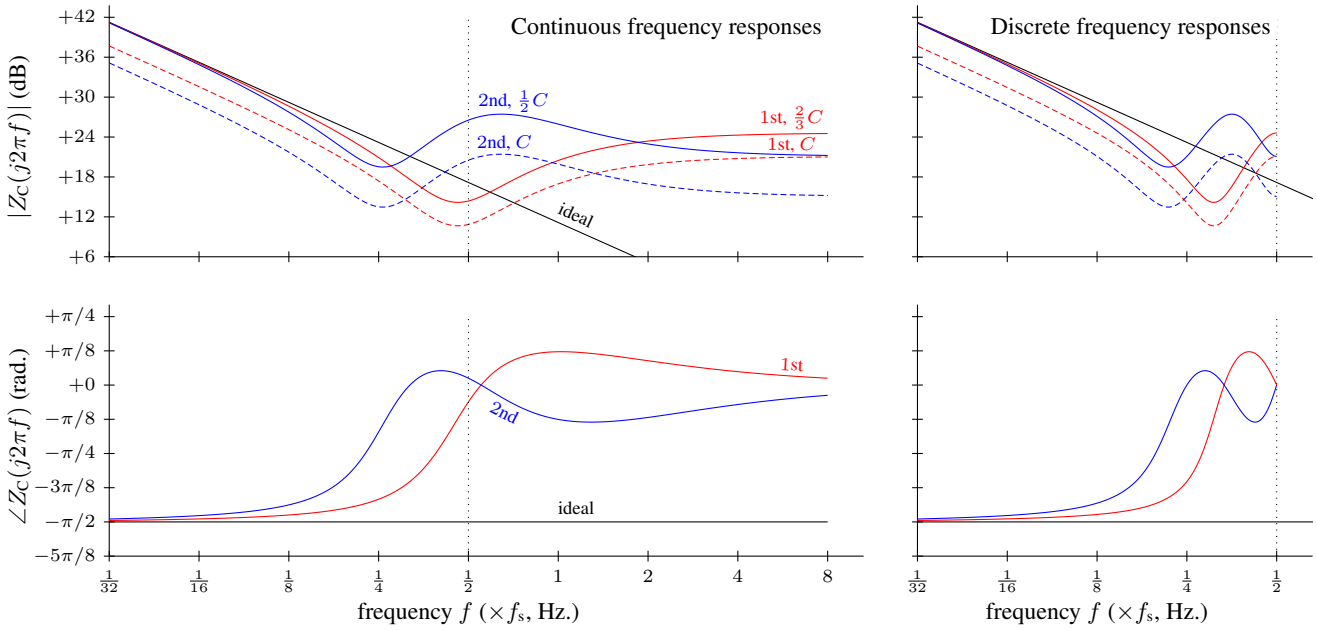

Figure 4: *Impedance of a standard capacitor, a capacitor treated with 1st-order ADAA, and a capacitor treated with 2nd-order ADAA. Capacitor value is $C = 1$ μF, sampling rate is $f_s = 44100$ Hz. Magnitude is shown in the top two panes, and phase is shown in the bottom two panes. The left two panes show continuous-time responses, and the right two panes compared discrete-time responses of the ADAA-treated filters to the ideal continuous-time response.*

5.4. What changes, T or C (resp. L)?

Now, we revisit $\tilde{C}$ (resp. $\tilde{L}$) and $\tilde{T}$. These should be set so that the "asymptotic" circuit as $T \longrightarrow 0$ matches the original capacitor C (inductor L), i.e., that the low-frequency impedance is correct. To illustrate this, Fig. 4 shows the magnitude and phase of the 1st-order ADAA'd capacitor (red, labelled "1st") and 2nd-order ADAA'd capacitor (blue, labelled "2nd"). Notice that setting $\tilde{C} = C$ (dashed red line) has a significant magnitude mismatch against the ideal capacitor ($Z = 1/Cs$) at low frequencies, which is corrected by setting $\tilde{C} = \frac{2}{3}C$ (solid red line) resp. $\tilde{C} = \frac{1}{2}C$ (solid blue line). This choice does not affect the impedance phases.

Hence, we argue that for 1st-order ADAA we should set capacitances to $\tilde{C} = \frac{2}{3}C$ (inductances to $\tilde{L} = \frac{2}{3}L$), for 2nd-order ADAA should set capacitances to $\tilde{C} = \frac{1}{2}C$ (inductances to $\tilde{L} = \frac{1}{2}L$), and that in all cases, we should have $\tilde{T} = T$.

Previous work that applied ADAA to stateful systems [17, 18, 20] instead argued that the sampling period T is adjusted by the introduction of ADAA, reasoning from the perspective of matching delays. We offer the discussion in this paper as an alternate explanation that is more tightly coupled to reasoning about an analog circuit prototype, that holds in the limit as $T \longrightarrow 0$ (where arguments about adjusting T would not hold), and that has the additional benefit of allowing us to still think in terms of the standard BLT, without considering any frequency warping in particular.

5.5. 1st-order vs. 2nd-order

It is known from the ADAA literature that 2nd-order ADAA suppresses aliasing more than 1st order [17, 18, 20]. Can we say anything about the linear behavior? Looking again at Fig. 4, it is worth mentioning that the 2nd order ADAA'd reactance diverges from the ideal at a lower frequency, and has more inflections in the magnitude and phase responses (possibly leading to more undesirable resonances). This means that 2nd-order ADAA probably requires more oversampling that 1st-order ADAA, and that any artifacts may be qualitatively different between the two flavors.

6. CONCLUSION

In this paper, we derived electronic circuits representing 1st- and 2nd-order antiderivative antialiasing, operating in the linear regime, applied to reactances. This gives a new analytical tool for studying ADAA filters, confirms the stability proof of [17, 18] from a new angle while extending it to 2nd-order, and gives a new perspective on warping circuit values rather than the sampling period. Future work could investigate higher-order ADAA [8, 10] or apply these concepts to state-space modeling.

7. ACKNOWLEDGMENTS

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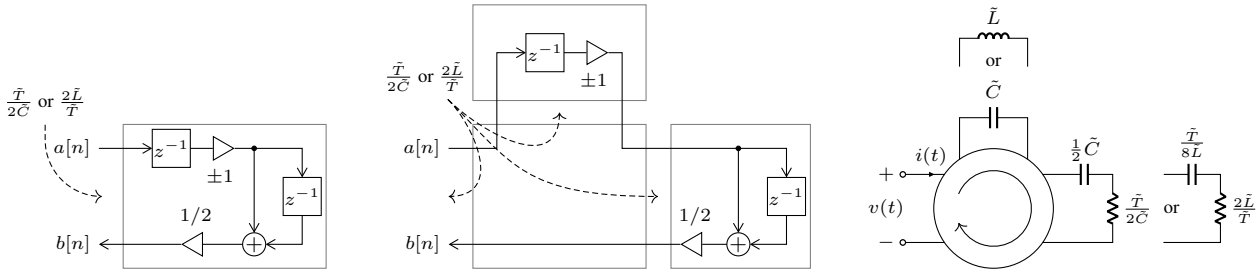
A. APPENDIX: BRUNE SYNTHESIS

In this paper, we've synthesized various RLC circuits from continuous-time impedances using Brune's method [29, 30]. To illustrate the process, we'll work one of these synthesis procedures in detail.

Recall the WDF capacitor with added ADAA filter derived in §3.2. Here, we'll illustrate the circuit synthesis procedure shown in Fig. 1. We start with an impedance

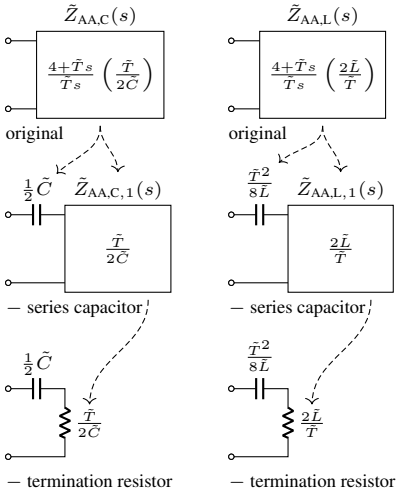
$$\tilde{Z}_{\mathrm{C}}(s) = \frac{8 + 2\tilde{T}s + \tilde{T}^2 s^2}{6\tilde{T}s + \tilde{T}^2 s^2} \frac{\tilde{T}}{2\tilde{C}}. \tag{31}$$

$\tilde{Z}_{\mathrm{C}}(s)$ has a pole at $s = 0$, telling us we can extract a series capacitor, which we'll call C_*, leaving behind a reduced impedance



(a) Capacitor / Inductor WDF. (b) Group to highlight structure. (c) Synthesize circuit.

Figure 5: *Alternate ways of synthesizing a circuit from the wave-domain ADAA capacitor or inductor.*



(a) Capacitor. (b) Inductor.

Figure 6: *Synthesizing a circuit from the wave-domain ADAA filter for a capacitor and inductor (on their own, without the capacitor or inductor themselves).*

$\tilde{Z}_{\mathrm{C},1}(s)$. The relationship between these impedances is

$$\tilde{Z}_{\mathrm{C},1}(s) = \tilde{Z}_{\mathrm{C}}(s) - \frac{1}{C_* s} \tag{32}$$

$$= \frac{8C_* + 2C_*\tilde{T}s + C_*\tilde{T}^2 s^2 - 12\tilde{C} - 2\tilde{C}\tilde{T}s}{12\tilde{C}C_* s + 2\tilde{C}C_*\tilde{T}s^2} . \tag{33}$$

The numerator order of $\tilde{Z}_{\mathrm{C},1}(s)$ can be reduced by solving

$$8C_* - 12\tilde{C} = 0 , \tag{34}$$

which is accomplished by $C_* = \frac{3}{2}\tilde{C}$. Extracting the series capacitor C_* leaves behind the impedance

$$\tilde{Z}_{\mathrm{C},1}(s) = \frac{2 + 3\tilde{T}s}{18 + 3\tilde{T}s} \frac{\tilde{T}}{2\tilde{C}} . \tag{35}$$

$\tilde{Z}_{\mathrm{C},1}(s)$ now has no zeros or poles at $s = 0$ or $s = \infty$, meaning it's time to extract either a series or parallel resistor. We'll handle the two cases separately, in the following two subsections.

A.1. Extracting shunt resistor

The shunt resistor option is shown on the left side of Fig. 1. Extracting a shunt resistor R_* leaves behind an impedance $\tilde{Z}_{\mathrm{C},2}(s)$. The relationship between these impedances is

$$\tilde{Z}_{\mathrm{C},2}(s) = \frac{R_*\tilde{Z}_{\mathrm{C},1}(s)}{R_* - \tilde{Z}_{\mathrm{C},1}(s)} \tag{36}$$

$$= \frac{2R_*\tilde{T} + 3R_*\tilde{T}^2 s}{36\tilde{C}R_* + 6\tilde{C}R_*\tilde{T}s - 2\tilde{T} - 3\tilde{T}^2 s} . \tag{37}$$

The denominator order of $\tilde{Z}_{\mathrm{C},2}(s)$ can be reduced by solving

$$6\tilde{C}R_*\tilde{T}s - 3\tilde{T}^2 s = 0 , \tag{38}$$

which is accomplished by $R_* = \frac{\tilde{T}}{2\tilde{C}}$. Extracting the shunt resistor R_* leaves behind the impedance

$$\tilde{Z}_{\mathrm{C},2}(s) = \frac{2 + 3\tilde{T}s}{16} \frac{\tilde{T}}{2\tilde{C}} . \tag{39}$$

$\tilde{Z}_{\mathrm{C},2}(s)$ has a pole at $s = \infty$, telling us we can extract a series inductor, which we'll call L_*, leaving behind a reduced impedance $\tilde{Z}_{\mathrm{C},3}(s)$. The relationship between these impedances is

$$\tilde{Z}_{\mathrm{C},3}(s) = \tilde{Z}_{\mathrm{C},2}(s) - L_* s \tag{40}$$

$$= \frac{2\tilde{T} + 3\tilde{T}^2 s - 32\tilde{C}L_* s}{32\tilde{C}} . \tag{41}$$

The numerator order of $\tilde{Z}_{\mathrm{C},3}(3)$ can be reduced by solving

$$3\tilde{T}^2 s - 32\tilde{C}L_* s = 0 , \tag{42}$$

which is accomplished by $L_* = \frac{3\tilde{T}^2}{32\tilde{C}}$. Extracting the series inductor L_* leaves behind the impedance

$$\tilde{Z}_{\mathrm{C},3}(s) = \frac{1}{8} \frac{\tilde{T}}{2\tilde{C}} . \tag{43}$$

$\tilde{Z}_{\mathrm{C},3}(s)$ has no dependence on s, so it is a termination resistor of value $\frac{\tilde{T}}{16\tilde{C}}$. This concludes the synthesis procedure.

A.2. Extracting series resistor

The series resistor option is shown on the right side of Fig. 1. As an alternative to extracting the shunt resistor, we can extract a series resistor R_*, leaving behind an impedance $\tilde{Z}_{\mathrm{C},2}(s)$. The relationship between these impedances is

$$\tilde{Z}_{\mathrm{C},2}(s) = \tilde{Z}_{\mathrm{C},1}(s) - R_* \tag{44}$$

$$= \frac{2\tilde{T} + 3\tilde{T}^2 s - 36\tilde{C}R_* - 6\tilde{C}R_*\tilde{T}s}{36\tilde{C} + 6\tilde{C}\tilde{T}s}\,. \tag{45}$$

The numerator order of $\tilde{Z}_{\mathrm{C},2}(s)$ can be reduced by solving

$$2\tilde{T} - 36\tilde{C}R_* = 0\,, \tag{46}$$

which is accomplished by $R_* = \frac{\tilde{T}}{18\tilde{C}}$. Extracting the series resistor R_* leaves behind the impedance

$$\tilde{Z}_{\mathrm{C},2}(s) = \frac{8\tilde{T}s}{54 + 9\tilde{T}s}\frac{\tilde{T}}{2\tilde{C}} \tag{47}$$

$\tilde{Z}_{\mathrm{C},2}(s)$ has a zero at $s = 0$, telling us we can extract a shunt inductor, which we'll call L_*, leaving behind a reduced impedance $\tilde{Z}_{\mathrm{C},3}(s)$. The relationship between these impedances is

$$\tilde{Z}_{\mathrm{C},3}(s) = \frac{L_*\tilde{Z}_{\mathrm{C},2}(s)s}{L_*s - \tilde{Z}_{\mathrm{C},2}(s)} \tag{48}$$

$$= \frac{8L_*\tilde{T}^2s^2}{108\tilde{C}L_*s + 18\tilde{C}L_*\tilde{T}s^2 - 8\tilde{C}\tilde{T}^2s}\,. \tag{49}$$

The denominator order of $\tilde{Z}_{\mathrm{C},3}(s)$ can be reduced by solving

$$108\tilde{C}L_*s - 8\tilde{C}\tilde{T}^2s = 0\,, \tag{50}$$

which is accomplished by $L_* = \frac{2\tilde{T}^2}{27\tilde{C}}$. Extracting the series inductance L_* leaves behind the impedance

$$\tilde{Z}_{\mathrm{C},3}(s) = \frac{8}{9}\frac{\tilde{T}}{2\tilde{C}}\,. \tag{51}$$

$\tilde{Z}_{\mathrm{C},3}(s)$ has no dependence on s, so it is a termination resistor of value $\frac{4\tilde{T}}{9\tilde{C}}$. This concludes the synthesis procedure.

B. APPENDIX: ALTERNATIVE WDF DERIVATION

In §§3–4, we used the wave variable transformation and inverse BLT to find a continuous-time impedance function corresponding the ADAA'd WDF capacitor, then finding a corresponding RLC circuit using Brune synthesis. This Appendix presents an alternative perspective, based on recognizing common one- and three-port WDF building blocks, and still a little bit of Brune synthesis. Here we only consider 1st-order ADAA for brevity.

B.1. Alternative capacitor derivation

Taking the $\pm$ as a $+$ and the port resistance as $\frac{\tilde{T}}{2\tilde{C}}$, Fig. 5a shows the signal flow graph of a WDF capacitor with an applied 1st-order ADAA filter. We know already this is formed by cascading an adapted WDF capacitor (a unit delay z^{-1} with port resistance $\frac{\tilde{T}}{2\tilde{C}}$) with the ADAA filter from Eqn. (5).

Recognizing that Fig. 5a has the structure of two cascaded filters of wave variables, we can pull out the cascading operation itself as a three-port element, as shown in Fig. 5b (again, taking the $\pm$ as a $+$ and the port resistance as $\frac{\tilde{T}}{2\tilde{C}}$). Then, we can ask ourselves: "What does cascading look like in the wave domain?" In fact, there is a standard three-port electrical element that does this: a *circulator* with identical port resistance at all three ports. The port resistance at the external port is already set to $\frac{\tilde{T}}{2\tilde{C}}$, which constrains its other two ports to have the same port resistance. This immediately gives us an interpretation of the unit delay as a capacitor of value $\tilde{C}$, discretized with the BLT.

Now, how can we interpret the ADAA filter, with port resistance $\frac{\tilde{T}}{2\tilde{C}}$? We again use the Brune synthesis procedure, as illustrated in Fig. 6a. Using the inverse BLT (2) on (5) yields a continuous-time reflectance

$$H_{\mathrm{AA}}(s) = \frac{2}{2 + \tilde{T}s}\,. \tag{52}$$

Recalling that the port resistance $Z_{\mathrm{AA}} = \frac{\tilde{T}}{2\tilde{C}}$, we can use (12) to find the continuous-time impedance

$$Z_{\mathrm{AA,C}}(s) = \frac{4 + \tilde{T}s}{\tilde{T}s}\left(\frac{\tilde{T}}{2\tilde{C}}\right)\,. \tag{53}$$

We now apply Brune synthesis, yielding the series combination of capacitor $\frac{1}{2}\tilde{C}$ and resistor $\frac{\tilde{T}}{2\tilde{C}}$ shown in Fig. 6a.

So, finally, we have found that the WDF capacitor plus ADAA filter can be viewed as a circulator terminated on a capacitor $\tilde{C}$ on one port, and the series combination of a capacitor $\frac{1}{2}\tilde{C}$ and a resistor $\frac{\tilde{T}}{2\tilde{C}}$ on the other port.[2] A disadvantage of this derivation, compared to the one presented in §3.2, is that it involves the slightly unusual electrical element of the circulator, which perhaps only microwave engineers are comfortable reasoning with. But, it has the advantage that it makes a clear distinction between the original capacitor ($\tilde{C}$) and the circuit elements that are added by the ADAA filter (the circulator, capacitor $\frac{1}{2}\tilde{C}$, and resistor $\frac{\tilde{T}}{2\tilde{C}}$), whereas in our earlier derivation, they are inextricable mixed together. Thinking back to our earlier discussion on how $\tilde{T}$ and $\tilde{C}$ should be set, this adds another layer of richness—because the capacitor and resistor that are part of the ADAA filter depend on the original capacitor $\tilde{C}$, it would appear that there is no adjusting the ADAA filter without adjusting the original capacitor itself.

B.2. Alternative inductor derivation

The inductor derivations shown in Fig. 5a–5c (taking the $\pm$ as a $-$ and the port resistance as $\frac{2\tilde{L}}{\tilde{T}}$) and Fig. 6b, proceeds exactly as for the capacitor. The derivation of the circuit for the ADAA filter itself starts identically, since it is the same filter as for the capacitor. Beyond the continuous-time reflectance, the different port resistance comes into play, and the Brune synthesis yields a different circuit, as illustrated in Fig. 6b. In fact, it is identical except that all the impedances are just scaled by $\frac{2\tilde{L}}{\tilde{T}}/\frac{\tilde{T}}{2\tilde{C}} = \frac{4\tilde{C}\tilde{L}}{\tilde{T}^2}$. However, despite this scaling, the filter still comprises a resistor and a capacitor—it is not the dual of the ADAA filter as applied to the capacitor. Still, when all four elements are combined (the two capacitors, resistor, and circulator), the resulting impedance is indeed the dual of the ADAA'd capacitor.

[2] From here we can derive the same continuous-time impedance (18).